REMARKS

The Final Office Action mailed February 1, 2005, has been received and reviewed. Claims 1, 2 and 13 through 18 are currently pending in the application. Claims 1, 2 and 13 through 18 stand rejected. Applicants have amended no claims herein, and respectfully request reconsideration of the application.

35 U.S.C. § 103(a) Obviousness Rejections

Obviousness Rejection Based on U.S. Patent No. 5,424,652 to Hembree et al. in view of U.S. Patent No. 5,764,650 to Debenham

Claims 1, 2, 13 and 16 through 18 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Hembree et al. (U.S. Patent No. 5,424,652) in view of Debenham (U.S. Patent No. 5,764,650). Applicants respectfully traverse this rejection, as hereinafter set forth.

> M.P.E.P. 706.02(j) sets forth the standard for a Section 103(a) rejection:
>
> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, **the prior art reference (or references when combined) must teach or suggest all the claim limitations.** The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). (Emphasis added).

The 35 U.S.C. § 103(a) obviousness rejections of claims 1, 2, 13 and 16 through 18 are improper because the elements for a prima facie case of obviousness are not met. Specifically, the rejection fails to meet the criterion that the prior art reference must teach or suggest all the claims limitations.

Applicants respectfully request that the Examiner carefully reconsider the specific elements of the Hembree reference that are cited in the Office Action and alleged to correspond with elements of the Applicants' claim elements. Specifically, the Office Action erroneously alleges that the "wire bond[ing] 26" of the Hembree reference is an equivalent to Applicants'

"contacting the substrate with probes". (Office Action, p. 3). Applicants vigorously disagree and maintain that ***WIRE BONDS 26 are NOT analogous to CONTACTING A SURFACE OF THE SUBSTRATE WITH PROBES.***

Applicants' invention and the Humbree reference, while both drawn to testing of a die, are distinguishable in that Applicants' invention is drawn to "directly detachably contacting the surface of the substrate with probes; . . . bringing the . . . die and the substrate together in conductive contact . . .; and . . . electrically testing the assembly using the probes." In contrast, the Humbree reference places the die and substrate within a cavity of a housing and wire bonds the substrate pad out to external leads on the housing which are "probed" during testing.

Specifically, the ***Office Action alleges***:

> ***Hembree et al anticipates*** a method for electrically testing a flip-chip semiconductor assembly formed from at least one integrated circuit (IC) die (24) and a substrate (14), the method comprising:
>
> ***Contacting the substrate with probes (26)***;
>
> While the substrate is in contact with the probes, bringing the at least one die and the substrate together (via metal clips 34) in conductive contact to form the flip-chip semiconductor assembly; and
>
> Before the at least one die is sealed, electrically testing the assembly using the probes (col 5, ln 19-47) as recited in claim 1.
>
> Although Hembree et al does not show directly detachably contacting a surface of the substrate with probes, Debenaham shows a method of *detachably contacting* a surface of a substrate with probes (col 3, ln 38-47 and col 6, ln 66 – col 7, ln 10). (Office Action pp. 2-3).

Applicants respectfully disagree with the characterization of the alleged teachings of the Hembree reference. Clearly, the steps of method claims are carried out through the interrelationship of elements. The Office Action introduced the Hembree reference and alleged that it teaches the step of "Contacting the substrate with probes (26)". (Office Action, p. 3). The only recitation of "26" within the Humbree reference is located at column 4, lines 19-23, which reads, "The insert traces 14B which terminated near the edge of the insert substrate 14A were ***wire bonded 26*** to the connection points 18 within the housing 10, and were therefore electrically coupled with leads 28 attached to the traces (not shown) on the exterior of the housing10." (Emphasis added.)

Claim language is interpreted according to the plain meaning of the term, the meaning given in the specification or the dictionary meaning depending upon the presence of such definitions. Accordingly, Applicants use of the term "probes" in the claim step "directly detachably contacting a surface of the substrate with probes" should be accorded such interpretations. Since the term "probes" was not redefined in Applicants' specification, the plain or dictionary meaning will control. Accordingly, according to Merriam-Webster's Online Dictionary (http://www.m-w.com/cgi-bin/dictionary?book=Dictionary&va=probes), the term ***"probes"*** is defined as "any of various testing devices or substances: as (1) **: *a pointed metal tip for making electrical contact with a circuit element being checked***". In contrast, the term "wire bonding" is a technical term that is not listed in conventional dictionaries. Therefore, Applicants provide a glossary definition from a well-respected technical text book for the term "***wire bonding***", namely, "***[a]n assembly step in which thin gold or aluminum wires are attached between the die bonding pads and the lead connections in the package.***" (*Microchip Fabrication-A Practical Guide to Semiconductor Processing*, McGraw-Hill, Peter Van Zant, 2nd Ed. (1990)). In short, the steps of "contacting . . . with probes" and "wire bonding" are not the same.

Applicants' invention as presently claimed in independent claim 1 reads:

> 1. A method for electrically testing a flip-chip semiconductor assembly formed from at least one integrated circuit (IC) die and a substrate, the method comprising:
> **directly detachably contacting a surface of the substrate with probes;**
> **while the substrate is in contact with the probes, bringing the at least one die and the substrate together in conductive contact** to form the flip-chip semiconductor assembly; and
> before the at least one die is sealed, electrically testing the assembly using the probes. (Emphasis added.)

In contrast to Applicants' invention as claimed, the Humbree reference specifically discloses:

> The insert traces 14B which terminated near the edge of the insert substrate 14A were wire bonded 26 to the connection points 18 within the housing 10, and were therefore electrically coupled with lead 28 attached to the traces

> (not shown) on the exterior of the housing 10 . . . [and] [t]he leads 28 allow for coupling of the package with a test fixture. (Col. 4, lines 19-27).
>
> After mating the bond pads 22 with the contacts 20, metal clips 34 held the lid 30 in place to prevent shifting of the lid 30, and therefore the die 24, during testing. (Col. 5, lines 19-21).
>
> Since the assembled package was similar to a conventional ceramic semiconductor package, a conventional test sequence, including burning in, was used to ensure functionality of the die. After the die was tested, the lid was removed from the package by removing the clips, and the die was removed from the lid. (Col. 5, lines 26-31).

Clearly, the ***Humbree reference discloses*** a substrate that is retained in a cavity in a housing. The substrate has contacts that are connected to traces on the substrate. The substrate traces are ***bonded*** to the housing using ***wire bonds*** 26 which, in turn, electrically connect to leads on the housing that are then coupled to test equipment during testing. ***A die with bond pads*** is then ***brought into electrical contact with the contacts on the substrate and retained in place by a lid which conceals any and all probe access to the substrate within the cavity of the housing.*** **In Humbree, the very act of bring the die into contact with the substrate prevents any access by a probe to the surface of the substrate.** Again, Humbree's "wire bonds 26" are not analogous to Applicants' "probes" nor are they capable of "directly detachably contacting a surface of the substrate with probes" as the substrate is inaccessible and completely forecloses the possibility carrying out Applicants' claimed act of "while the substrate is in contact with the probes, bringing the at least one die and the substrate together in conductive contact".

Regarding the introduction of the Debenham reference, the Office Action stated that the Hembree reference anticipated the step of "Contacting the substrate with probes (26)", the Office Action introduces the Debenham reference, stating:

> Although Hembree et al does not show directly *detachably contacting* a surface of the substrate with probes, Debenham shows a method of detachably contacting a surface of a substrate with probes (col 3, ln 38-47 and col 6, ln 66-col 7, ln 10). (Office Action, p. 3).

Applicants assume that the specific citations "teach" some form of "detachably contacting" as alleged in the Office Action, however, nothing in the citations discuss any form of contacting in any type of detail. Applicants, for the Examiner's convenience, recite the specific

Debenham citations in full as evidence of lack of any specificity that would provide any teaching of the lacking elements, not to mention the lack of any motivation or suggestion to combine. Specifically, Debenham reads:

> The present invention relates to a system and method for testing a semiconductor device. The semiconductor device may be any of a variety of devices including, but not limited to, a chip on a wafer, a bare chip off a wafer, a packaged chip including a package and leads. The chip may perform any of a variety of functions including but not limited to memory, microprocessor, and ASIC functions. Further, the system and method may involve testing more than one semiconductor device at a time. (Debenham, col 3, ln 38-47)

> Referring to FIG. 2, testing assembly 14 includes a tester 46 that performs tests on semiconductor devices. The semiconductor devices each may be any of a variety of devices including, but not limited to, a wafer, chips on a wafer, bare chips off a wafer, or packaged chips including a package and leads. Merely as an example, semiconductor devices 50A and 50B (collectively semiconductor devices 50) are each packaged chips including leads, and semiconductor devices 52A and 52B (collectively semiconductor devices 52) are each wafers having numerous chips (or dice). The equipment of testing assembly 14 is preferably automated test equipment. (Debenham, col 6, ln 66-col 7, ln 10)

Nothing in the Debenham reference provides any of Appliants' claimed elements that are lacking in the Hembree reference. Therefore, independent claim 1, and claims 2, 13 and 16-18 depending therefrom, are clearly allowable over the cited prior art of the Hembree reference in view of the Debenham reference under 35 U.S.C. § 103. Accordingly, such claims are allowable over the cited prior art and Applicants respectfully request that such rejections be withdrawn.

Obviousness Rejection Based on U.S. Patent No. 5,424,652 to Hembree et al. in view of U.S. Patent No. 5,764,650 to Debenham as applied to claim 1 above, and further in view of U.S. Patent No. 5,701,233 to Carson et al.

Claims 14 and 15 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Hembree et al. (U.S. Patent No. 5,424,652) in view of Debenham (U.S. Patent No. 5,764,650) as applied to claim 1 above, and further in view of Carson et al. (5,701,233). Applicants respectfully traverse this rejection, as hereinafter set forth.

M.P.E.P. 706.02(j) sets forth the standard for a Section 103(a) rejection:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, **the prior art reference (or references when combined) must teach or suggest all the claim limitations.** The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). (Emphasis added).

The 35 U.S.C. § 103(a) obviousness rejections of claims 14 and 15 are improper because the elements for a prima facie case of obviousness are not met. Specifically, the rejection fails to meet the criterion that the prior art reference must teach or suggest all the claims limitations.

Regarding claim 14, which depends from independent claim 1, and claim 15 depending from claim 14, Applicants sustain the above-proffered arguments that Hembree reference in view of the Debenham reference do not teach, disclose or motivate Applicants' invention as claimed in independent claim 1. The Office Action introduces the Carson reference and alleges:

> . . . Carson et al shows the use of epoxy dots (Figures 14a and 14b) on one of the bond pads on the at least one IC die and the conductive pads on the substrate (col 10, ln 52-62), as mentioned in claim 14. Moreover, Carson et al further emphasizes flip-chip bonding (col 7, ln 35-38) as also mentioned in claim 1.
>
> As to claim 15, the use of conductive epoxy dots being one of wet or dry type is considered inherent to any conductive epoxy dot because the epoxy dots can only be made of a wet or dry type composition. (Office Action, pp. 4-5).

Even assuming arguendo, that the Carson reference teaches epoxy dots, neither the Hembree, Debenham nor Carson references, either individually or in any proper combination, teach, disclose or motivate Applicants' invention as claimed in the base independent claim 1, namely:

> 1. A method for electrically testing a flip-chip semiconductor assembly formed from at least one integrated circuit (IC) die and a substrate, the method comprising:
> **directly detachably contacting a surface of the substrate with probes;**
> **while the substrate is in contact with the probes, bringing the at least one die and**

the substrate together in conductive contact to form the flip-chip semiconductor assembly; and

before the at least one die is sealed, electrically testing the assembly using the probes. (Emphasis added.)

Therefore, Applicants respectfully request that the rejection of dependent claims 14 and 15 be withdrawn.

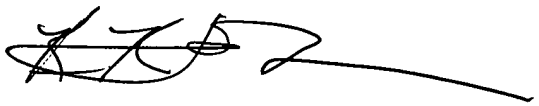
ENTRY OF AMENDMENTS

No claims have been amended herein. Further, Applicants' remarks do not raise new issues or require a further search. Finally, if the Examiner determines that the response does not place the application in condition for allowance, entry is respectfully requested upon filing of a Notice of Appeal herein.

CONCLUSION

Claims 1, 2, and 13 through 18 are believed to be in condition for allowance, and an early notice thereof is respectfully solicited. Should the Examiner determine that additional issues remain which might be resolved by a telephone conference, he is respectfully invited to contact Applicants' undersigned attorney.

Respectfully submitted,



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